Karlsruher Institut für Technologie

ITIV

Examination SS 2014

Communication Systems and Protocols

Prof. Dr.-Ing. Dr. h. c. Jürgen Becker ▪ Dr.-Ing. Alexander Klimm

Communication Systems and Protocols
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Name: «Vorname» «Nachname»
Matriculation ID: «Matrikelnummer»
ID-No.: «LaufNr»

Lecture Hall: «HS»
Seat No.: «PlatzNr»

Institut für Technik der Informationsverarbeitung (ITIV):
Prof. Dr.-Ing. Dr. h. c. Jürgen Becker
Prof. Dr.-Ing. Klaus Müller-Glaser
Prof. Dr. rer. nat. Wilhelm Stork

Engesserstr. 5

76131 Karlsruhe

Prerequisites for the examination

Aids

- Allowed aids for the examination are writing utensils, a ruler, a non-programmable calculator and a single sheet of A4 paper with self- and hand-written notes. Writing may be on a single side of the paper only. The use of own concept paper is not allowed.
- Use only indelible ink - use of pencils and red ink is prohibited.
- Other material than that mentioned above, is strictly forbidden. This includes any type of communication to other people.

Duration of the examination

120 minutes

Examination documents

The examination comprises 31 pages (including title page). Answers may be given in English or German. A mix of language within a single (sub)-task is not allowed. In your solution mark clearly which part of the task you are solving. Do not write on the backside of the solution sheets. If additional paper is needed ask the examination supervisor.
You will not be allowed to hand in your examination and leave the lecture hall in the last 30 minutes of the examination.
At the end of the examination: Stay at your seat and put all sheets into the envelope. Only sheets in the envelope will be corrected. We will collect the examination.

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Task 1 Cyclic Redundancy Check

Task 1.1 CRC-Calculation

The bitstream 1011101000 shall be coded and transmitted using the generator polynomial $g(x) = x^5 + x^4 + x^2 + 1$.

A) Determine the bitstream as it is being transmitted. 5

Bitstring for generator polynomial: 110101

Degree of generator polynomial = 5, therefore five zeros are appended to the bitstream

```
101110100000000: 110101 = 1100011101
110101
0110111
 110101
 0000100000
     110101
     0101010
      110101
       111110
       110101
         101100
         110101
        011001 ← Remainder
```

Bit stream as it is being transmitted: 101110100011001

A: 1pt: correct generator polynomial
B: 1pt: bitstream appended with five 0's
C: 2pts: calculation fully correct (per error -1pt)
D: 1pt: correct bitstream that is being transmitted

Remarks: if a too short polynomial has been used contact Jens or Alex

Task 1.2 CRC-Error Detection

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Given are the two generator polynomials:

1. $G_1(x) = x^5 + x^2 + 1$
2. $G_2(x) = x^5 + x^4 + x^2 + 1$

The data 10011011 should be secured for any odd number of errors. Which polynomial from these two would you choose? Justify your answer.

REASONING VIA FACTOR (X+1). IF IT IS CONTAINED WITHIN THE POLYNOMIAL THEN ODD NUMBER OF ERRORS CAN BE DETECTED:

G_1:

$x^5 + x^2 + 1 : (x+1) = x^4 - x^3 + x^2 + (1 / (x+1))$ has a remainder, therefore x+1 is not contained

G_1 can not detect any odd number.

G_2:

$x^5 + x^4 + x^2 + 1 = (x + 1) (x^4 + x + 1)$ has no remainder. X+1 is contained

G_1 can detect any odd number.

SOLUTION USING EXAMPLES:

G1: counterexample is given with odd number of errors that are not detected

G2: calculate examples with 1 error, 3 errors, 5 errors and 7 errors and show that in all cases errors are detected!

Reasoning via factor (x+1):
1 pt G1 cannot detect odd number errors
1 pt for calculation/reasoning for G1

1 pt G2 can detect odd number errors
1 pt for calculation/reasoning for G2

Reasoning using examples:
1 pt G1 cannot detect odd number errors
1 pt for calculation of one counterexample for G1

1 pt G2 can detect odd number errors
1 pt for calculation of all (!) odd errors (1, 3, 5, 7) for G2)

Task 1.3 Parity Check

For protection of a block transmission parity bits are used as checksum. Blocks of always 8 bytes are protected by adding a parity bit for every byte and by adding additional parity bits for each column. **Even** parity is used.

A) What different type of errors can always be detected using block checking when using the protection scheme depicted above? Name three error types. **1**

Burst errors (not longer than 9 bits)

And odd number of Single bit errors

Even bit errors that are not distributed in a rectangular formation

1 pt for 3 correct answers
0.5 pts for 2 correct answers

B) What types of errors can ALWAYS be corrected using block checking? Name two. **1**

Single bit errors

Burst Errors under certain assumptions (only one error per block, length not a multiple of 9)

2 bit errors

0.5 pt: Single errors
0.5 pt: Burst Errors (it must be made clear that not all burst errors are detectable)

C) The following data was received. Check the parity bits and mark the bits that are interpreted as erroneous. **2**

	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7	Parity
Byte 0	0	0	1	0	1	1	1	1	1
Byte 1	1	1	0	1	0	1	1	0	1
Byte 2	0	1	0	1	0	1	0	0	0
Byte 3	0	1	1	1	1	0	1	1	1
Byte 4	1	1	1	0	0	0	0	1	1
Byte 5	0	0	0	0	1	0	1	1	1
Byte 6	1	1	1	0	0	0	0	1	0
Byte 7	1	0	0	1	1	0	1	0	0
Parity	0	1	1	0	0	1	1	1	1

2 pt: all correct bits marked OR
1 pt: all parity checks done correctly
0,5: at least two parity checks correct

D) Is this information enough to reconstruct the original data? If yes give the original bytes that were sent. If no, give reason why this is not possible? **1**

It is not possible because other errors might have gone unnoticed (4 single bit errors in Rectangular formation)

No point for only yes/no
0.5 pts when reasoning is wrong

Task 1.4 General Questions

A) The communication in a system consisting of a sensor, a connection and a microcontroller shall be secured for errors. The sensor measures 28 bytes of data every 20 ms that should be sent in one transfer. The bandwidth of the connection is 13000 bit/sec. For the error detection the choice is between CRC16, CRC32, CRC64 and a block code that protects eight bit per row. What error protection is implementable in the given system? **2**

224 bits of data every 20ms. 50 data transfers per second are possible.

With given bandwidth, a maximum of 260 bits per transfer are possible:
13000 bit/sec : 50 transfers/sec = 260 bit/transfer

Overhead: crc16 -> 16 bit, crc32 -> 32 bit, crc64 -> 64 bit -> block code: 37 bit

Total bits per transfer: crc16 -> 240 bit, crc32 -> 256 bit, crc64 -> 288 bit -> block code: 261 bit

Required transmission rate including overhead:

CRC16: 12000 bit/s

CRC32: 12800 bit/s

CRC64: 14400 bit/s

Block Code: 13050 bit/s

A: +0.5 pts: reasoning over bandwidth of data connec
B: +0.5 pts: correct overhead of crc (all types)
C: +0.5 pts: correct overhead of block code
D: +0.5 pts: All implementable schemes

CRC 16 and CRC 32 can be implemented because only a maximum rate of 13000 bit/sec is available

B) Name three possible ways for error handling and sort them by the amount of overhead added to the communication in the case of a single bit error. Assume 128 bit of data that should be sent over a bus and additional redundant bits that can be used to protect the data. Justify your answer; an estimation of the overhead is sufficient. **2**

Discard data: overhead to detect error (can be CRC, but parity would be enough), but data is lost

Correction: additional bits to correct the values (HD = 2), more needed than only for detection

Resend: overhead to detect error, report error back to sender and resend data. Sending the data again creates more overhead than being able to correct a single bit error.

A: +1 pt: three correct error handling
B: +0,5 pts: correct order (increasing/decreasing overhead)
C: +0,5 pts: for estimation of overhead

Task 2 Media Access

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Task 2.1 Transmission

A) Name two different types of transmission according to their direction and explain them shortly. 2

Simplex single direction

Half-Duplex both direction, NOT simultaneously

Full-Duplex bidirectional

(Only two types needed)

0,5 per Type
0,5 per Explanation

Task 2.2 Multiple use of media

A) Name four different types of Multiplexing schemes. Explain them shortly. 2

Space Devision (SDMA) use of multiple physical lines

Time Devision (TDMA) use of time slots

Frequency Devision (FDMA) use multiple frequencies at same location

Code Devision (CDMA) distribution over a wide spectrum -> spreading code

0,5 Per Type AND Explanation

B) How many Walsh-functions are needed for the simultaneous transmission of several Nodes? Give a formula depending on N Nodes or explain. 1

$$2^{\lceil ld(N) \rceil}$$

1 Point for Formula or correct Explanation

Explanation: 2 to the power of round up logarithm dualis of N

C) Calculate the Walsh-functions for a transmission of four nodes, using the substitution scheme 0 = +1 and 1 = -1.

1

Function 1	+1	+1	+1	+1
Function 2	+1	-1	+1	-1
Function 3	+1	+1	-1	-1
Function 4	+1	-1	-1	+1

Point only given for correct table
CAREFUL: Order can be different

ALSO correct:
-1 = 0
+1 = 1

Be careful for the next task (no forward errors)

Table 2.1: Walsh Functions

For a CDMA access scheme three chips of each Walsh-function from the subtask above got lost. Sending the bits listed in Table 2.2 the signal **0 0 -4 0** can be measured on the medium.

Node	send bit
A	**1**
B	**0**
C	**1**
D	**0**

Node	Original Walsh-function			
A	+1	+1	-1	**-1**
B	+1	**-1**	+1	-1
C	+1	**-1**	-1	+1
D	+1	+1	+1	**+1**

Table 2.2: CDMA scheme using Walsh-functions

D) Complete Table 2.2 with the correct Walsh Functions that are used by the nodes. Justify your answer by giving all your calculation steps or your complete reasoning.

4

+1 +1 +1 +1

0 0 -4 0

0 0 -4 0 Only fits to Node D (fourth Bit = +1, all other Nodes have a -1 somewhere) => 0 was sent inverted

+1 -1 +1 -1

0 0 -4 0

0 0 -4 0 0 was send, see above

third bit of Walsh is -1 and 0 was send, therefore has to be node B

+1 +1 -1 -1

0 0 -4 0

0	0	4	0	1 was send
				Third bit of Walsh is +1 and 1 was send, therefore has to be node A
+1	-1	-1	+1	
0	0	-4	0	
0	0	4	0	1 was send
				Last open Node is C

2nd solution:

Function 1 only fits to Node D, because of all chips being +1

Therefore a 0 has been sent Inverted to get the Signal -4 within the third chip

With a 0 beeing sent inververted Function 0 (third chip is +1) has been used by node B also sending 0

Therefore Functions 3 and 4 have been used to send a 1:

Function 3 has a +1 at the third chip. This could only be used by node A
Function 4 is left to Node C

A:	***1 Pts:***	***Fit Function 1 to node D because of +1 at all chips.***
B:	***1 Pts:***	***assignment of Sending 0 uses inverted Functions***
C:	***0,5 Pts***	***Fit Function 2 to Node B***
D:	***1 Pts:***	***Fit Functions 3 and 4 to correct Nodes depending on Chips***
E:	***0,5 Pts:***	***write original non-inverted Functions into Table 2.2***

ERRORCASE 1 – Table contains actual chips that are send (instead of Original Walsh function)

Step 1: Check for Column Values

Column 3 has to sum up to -4 (all rows have -1 there)
Column 2 has to sum up to 0 (row1 and row 4 have +1 there)

Conclusion for Step 1:

Node A uses function 3 (original function), because no other original function or inverted functions with "- / +1 / -1 / -1" exists.
Therefore '1' is encoded with original Walsh Function and '0' is encoded with inverted Walsh function

Step 2

Node C uses function 4 (no other function "- / -1 / -1 / -" exists)
Node B uses function 1 (no other inverted function "- / -1 / -1 / -" exists)
Node D uses function 2 (only Walsh function left)

F: 1 Pts: Ansatz with -4 and 0
G: 1 Pts: correct assignment of Node A
AND conclusion that '1' uses original function and '0' inverted Walsh function
H: 1 Pts: correct assignment of other functions (with reasoning)

ERRORCASE 2 – (Pre-)Assumption that '1' is encoded with inverted Walsh Function

+1 +1 +1 +1

0 0 -4 0

0 0 -4 0 Function 1 is sending '1'

Therefore either Node A or Node C are assigned to Function1

+1 -1 +1 -1

0 0 -4 0

0 0 -4 0 0 Function 2 is sending '1'

Therefore either Node A or Node C are assigned to Function2

Assignment of functions to the table is not possible, because the inverted Function 1 does not fit in the given Table

K: 0,5 Pts: Calculation of Function 1
L: 0,5 Pts: Calculation of Function 2
M: 1 Pts: Assignment not possible with reasoning

Task 2.3 Arbitration

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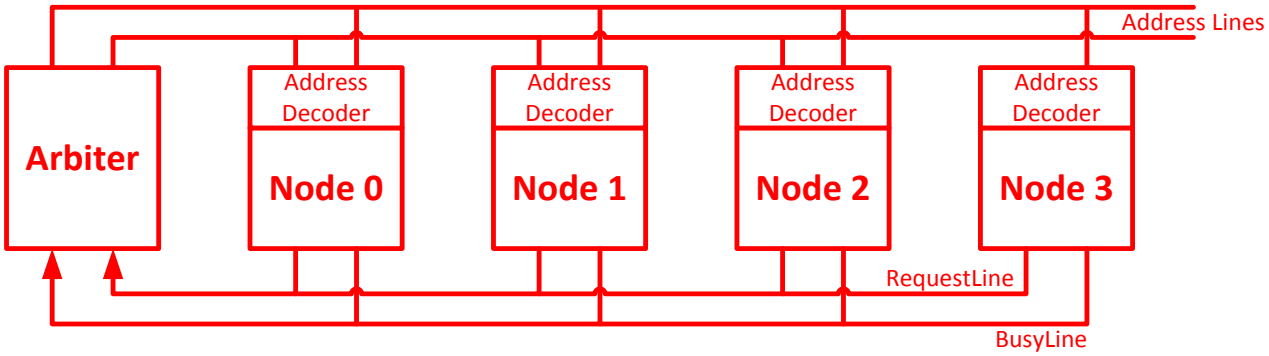
A) For the arbitration of four nodes a Polling model is used. Draw a Polling model with four nodes using an extra centralized Arbiter.
Label all used signals. Give a short explanation (one sentence) of each of the different types of signals used in this scheme. Mark the arbiter in your scheme and briefly explain its basic function (ca. 3 sentences).



Request: If node wants to send, it signalize it with the Request line

Address Lines: arbiter sequentially sets addresses on the lines to poll the nodes

Busy: if set by a node, the arbiter stops polling

A: 1 pt: figure of generally correct Polling model

Amount of Address Lines is not important -> naming and explanation gives points

B: +1 pt: explanation of all signal lines
OR
+0,5 pt: explanation of 2 signal lines

Node signalizes his request on the request line. The arbiter polls Nodes regarding their priority by sending the nodes' addresses. If node requested the bus and is polled, it sets the busy line and takes the bus. If busy line is set, the arbiter stops polling

C: 1 pt: for correct description

A system with four nodes is using a wired-AND CSMA/CA scheme to determine the order of the transmission. The identifiers of the nodes are as follows:

	LSB									MSB
Node 0:	0	1	0	0	1	0	1	0	0	0
Node 1:	1	0	1	1	0	1	0	1	0	0
Node 2:	1	1	0	1	0	0	0	1	1	0
Node 3:	0	0	1	1	1	0	1	0	0	0

Table 2.3: CSMA/CA Node Identifiers

B) Draw the signal flow for the arbitration if all nodes want to send a message simultaneously. The nodes start the transmission by sending the identifiers of Table 2.3. **3**

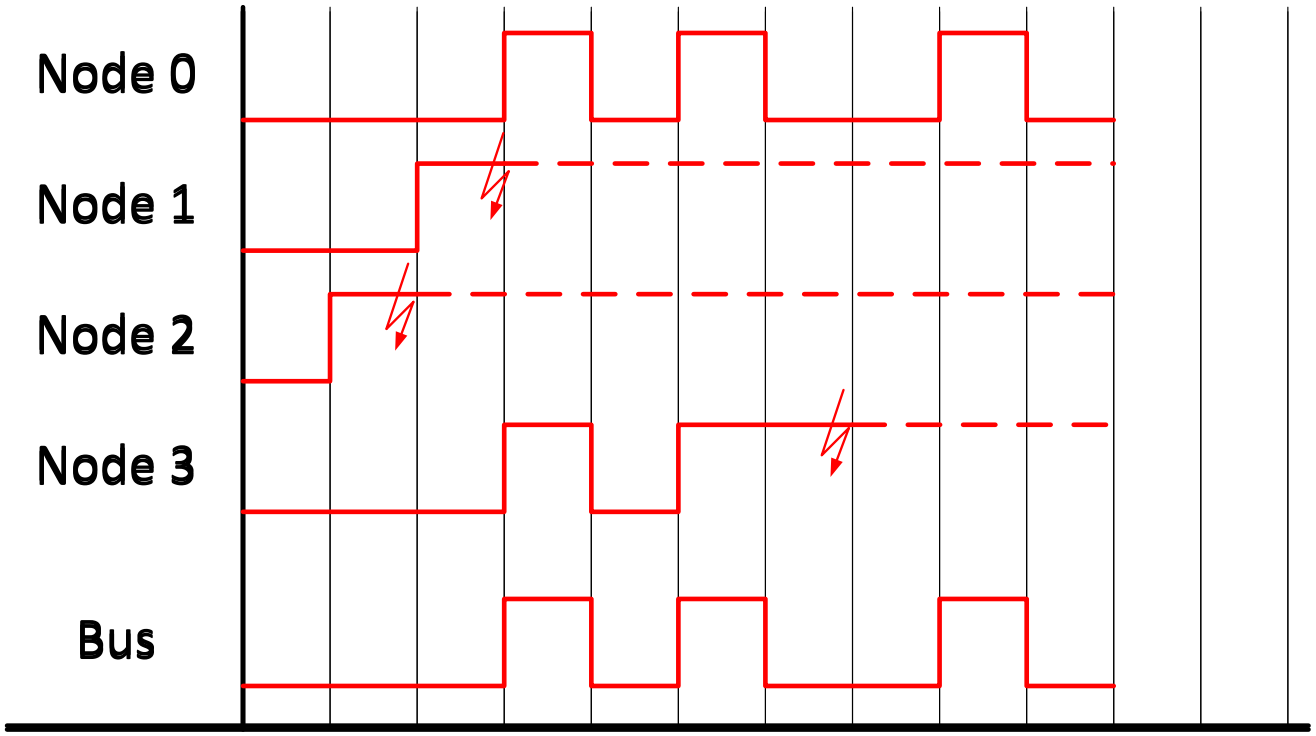


Figure 2.1: Signal flow for CSMA/CA

A: + 0,5 pts: if MSB is sent first
B: + 0,5 pts: per correct Line of Node 0, 1, 2, 3 and Bus line

The arbitration loss can be marked using a constant or dotted line a high level, or drawing no line at all. Drawing a line at low-level is wrong

Task 3 Synchronization

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Task 3.1 General Questions

A) An Ethernet connection uses a 4B5B line code. What is the purpose of the code? 1

Bit synchronization

B) Why is synchronization required during a data transfer? 1

Correct bit and frame boundary identification is required by the receiver for a successful message decoding. The purpose of synchronization is to provide these boundaries.

+1pt: detect bit- and/or frame bounderies

C) Name three synchronization methods and explain them shortly. 1

- Separate clock line
- Suitable line code
- Synchronized local clocks
- Clock recovery
- Bitstuffing
- Handshake signals
- Start / Stop
- Preamble
- Separate start/stop signal line (e.g. Chip Select for SPI)
- Appropriate line code

Task 3.2 Synchronization in Serial Communication

The lighting equipment on a stage is controlled via a serial communication connection running at 250KBit/s in 8N2 mode. 8N2 means that each transmitted byte is preceded by one start bit and succeeded by two stop bits.

Data on the serial connection is transmitted in frames with a fixed composition:

Each frame starts with a break (a low level on the signal line) with a length of 88 µs and a following mark (a high level on the signal line) of 8 µs. Subsequently one byte of header follows and finally 512 bytes of data are transmitted. (Hint 1KBit = 1000 Bit)

A) Calculate the maximum rate at which frames can be transmitted. 2

Bit time: 1 / 250 KBit/s = 4 µs

Byte time: (8+3) * 4 µs = 44 µs

Frame time: 88 µs + 8 µs + (513 * 44 µs) = 22668 µs = 44.115 Hz

+1pt: Ansatz of Frametime calculation
+1pt: correct result

Each node of the lighting equipment required to receive the serial data signal contains a microcontroller for this task. A typical microcontroller peripheral used to receive a serial signal is a UART. Normally it uses 16x oversampling of the signal line to eliminate any unwanted glitches.

B) Calculate the minimum operation frequency of the microcontroller when it is required to receive the serial data signal from above with its internal UART. **1**

250 Kbit/s * 16 = 4 MHz

A simpler serial receiver performs only 6 time oversampling. It takes three consecutive samples in the middle of each bit. A majority voting is used to determine the final bit value. The following diagram shows the serial signal at the receiver while a noisy header byte is received.

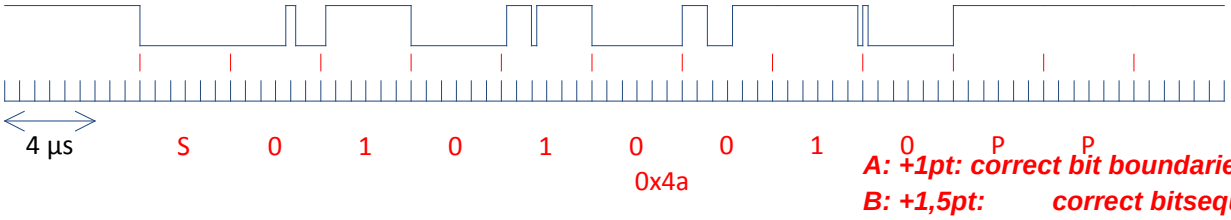

Figure 3.1: Signal flow for CSMA/CA

A: +1pt: correct bit boundaries and S/P
B: +1,5pt: correct bitsequence
(for each wrong bit -0,5 pts)
C: +0,5pt: HEX conversion

C) Mark the bit boundaries and determine the received bit values. Finally determine the received header byte in hexadecimal representation. (Hint: Bytes are transmitted LSB first.) **3**

0x4a

D) What is the maximum allowed duration of a glitch in the received signal when an error free reception of the signal is required? Use the receiver specification from the previous task (250 Kbit/s, 6x oversampling, 3 consecutive samples) and give all calculation steps. (Hint 1KBit = 1000 Bit) **2**

A: +1pt: Ansatz (1 sample out of 3 may be erroneous)
B: +1pt: correct glitch duration

250 KBit/s -> 4 µs bit time

6x oversampling ratio -> 0.666 µs sampling time

One out of three consecutive samples per bit might be erroneous

-> Maximum glitch duration: 0.666 µs

E) Fast and modern interface standards like e.g. PCI-Express or SATA predominantly use serial communication techniques. Name three advantages over a parallel communication? **2**

1. No Signal skew between multiple data lines is to be controlled
2. No Mutual disturbance of parallel data signals
3. Easy clock recovery is possible
4. Lower cost (cable, transceiver)
5. Scalable (Erweiterbar)

2pt: 3 correct advantages named
OR
1pt: 2 correct advantages named

F) Typically in high speed serial communications a 4B5B code or something similar is used. Name and explain an advantage over the Start-Stop Method previously discussed. **1**

1. DC free
2. Better clock recovery due to more available signal edges
3. Less protocol overhead
4. Some transmission errors can be detected

Task 4 Data Transmission

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Task 4.1 General questions

A) How does baseband differ from broadband? Name two differences. 1

Baseband	Broadband
Digital signals	Analog signals
Single channel that uses the entire bandwidth	Each transmission is assigned to a portion of the bandwidth
Frequency-division multiplexing is not possible	Multiple transmissions are possible at the same time
Bidirectional communication (same channel can be used to send and receive signals)	Unidirectional communication (to send and receive, two pathways are needed)

Task 4.2 System bit

A) The bandwidth of a video signal is 4.5MHz. This signal is to be transmitted using PCM (Pulse code modulation) with the number of quantization levels Q=1024. The sampling rate should be 20% higher than the Nyquist rate. Calculate the system bit rate. 2

Bandwidth W=4.5MHz

Nyquist rate f = 2*W = 9MHz but f should be 20% higher → f= 1.2*2*W =10.8MHz

$Q = 2^N = 1024$ with N=10

System bit rate r = N * f = 10 * 10.8MHz = 108 MBits/sec

A: +0,5pt regard Nyquist theorem
B: +0,5pt:calculate with 20% higher frequency
C: +0,5pt: use N=10
D: +0,5pt: Endresult is correct
No "Folgefehler"!

Task 4.3 Line Codes

A) Explain the Manchester Code encoding schemes and name one general application where it is applied. 2

1. The data are represented not by logic 1 or 0, but with line transitions.
   a. A logic 0 is represented by a transition from high to low, and a logic 1 is represented by a transition from low to high
   b. The coding occurs on every falling edge of the clock
2. Ethernet
3. ASI

A: +1pt: Explanation
B: +1pt: example (point only given together with explanation)

B) Draw the digital signals for the bit string 010 101 111 000 011 using each of the NRZ, Manchester, and differential Manchester digital encoding schemes. Label the bit values that are sent within each encoding diagram. **4**

A: +1pt: NRZ drawing correct

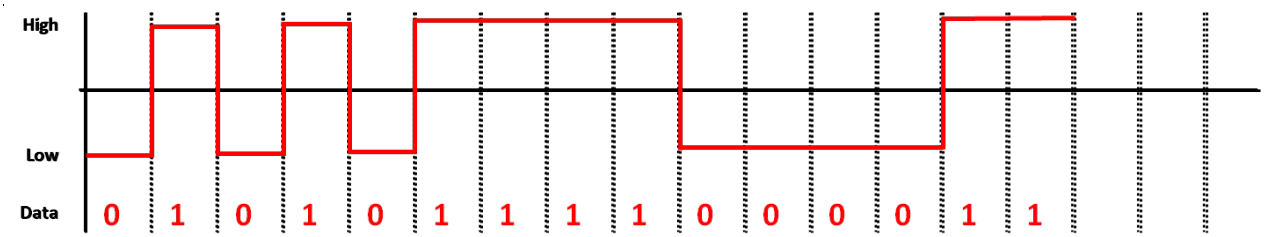


Figure 4.1: NRZ

B: +1pt: Manchester generally correct (level change in middle of bitvalue

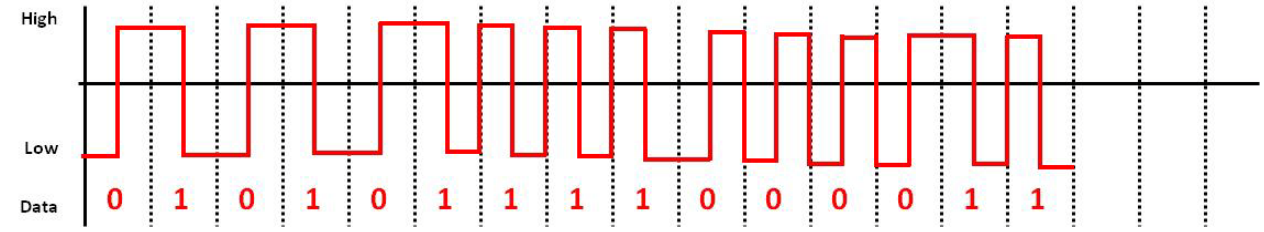


Figure 4.2: Manchester Code

C: + 1pt: Manchester with rising edge, differential Manchester with falling edge

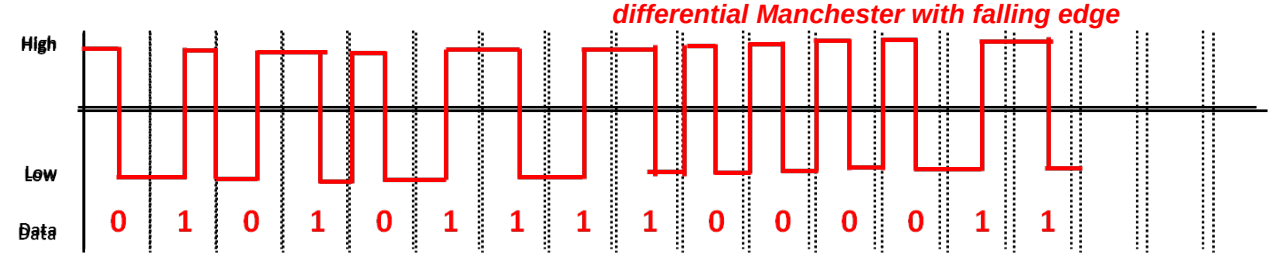


Figure 4.3: Differential Manchester Code

D: + 1 pt: bit values given in diagrams

C) Name three important properties of line codes. **2**

1. Error detection
2. Required Bandwidth
3. Timing Recovery
4. Direct Current Component
5. Number of collectively coded symbols

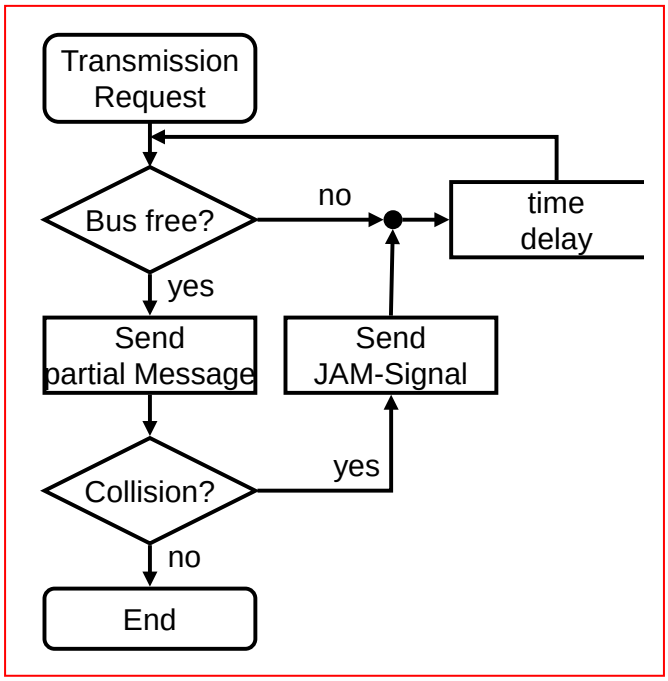
1pt: 2 correct properties
OR
2 pt: 3 correct properties

Task 4.4 Arbitration

A) Name one common known application where CSMA/CD protocol is applied? **1**

Access method used primarily with LANs configured in a bus topology (for example Ethernet)

B) Draw a sequence diagram (flowchart) of one node transmitting a message using the CSMA/CD protocol and explain each step in one sentence. **4**



A: +1pt: listen for free medium
B: +1pt: detection if collisions occur
C: + 1pt: collision detection is done continuously
D: + 0,5 pt: stations send out JAM signal when collision detected
E: + 0,5 pt: resend after random waiting time

No points without explanation

Stations monitor (listen to) the line to determine if the line is busy.

Any station (node) can send a message to any other station (or stations) as long as the transmission medium is free of transmissions from other stations.

If the station has a message to transmit but the line is busy, it waits for an idle condition (delay time) before transmitting its message.

If two stations transmit at the same time, a collision occurs. When this happens, the station first sensing the collision sends a special jamming signal to all other stations on the network. All stations then cease transmitting (back off) and wait a random period of time before attempting a retransmission.

If successive collisions occur, the back off period for each station is doubled. The random delay time for each station is different, and therefore, allows for prioritizing the stations on the network.

C) Name two advantages and two limitations of CSMA/CD protocols. **1**

Advantages	Disadvantages
simple scheme	- channel can be blocked because of many transmission requests
easy to extend	- bad efficiency in terms of bandwidth usage
	- data destruction
	- no real-time

1pt: for two advantages and two disadvantages
OR
0,5pt: for at least two correct advantages/disadvantages

Task 4.5 Corrupted clock lines

A) Given is an asynchronous communication system with one data line and one clock line. Data is transmitted using NRZ encoding. If the clock line is corrupted, is it still possible to transfer data? Justify your answer. **2**

Yes. By changing either to a data encoding enabling some kind of clock recovery.

OR

Yes. By changing the hardware in the nodes. For example:

1. Each node needs its own clock generator or
2. Edge detection and phase locked CRC at receiver side

OR

No. Under the assumption that NRZ encoding must be used it is necessary to have the same and synchronized clock on both sides. Therefore appropriate hardware has to be provided to ensure it. (either a clockline or local clocks that are synchronized for a transmission and are stable for the course of the transmission)

2pt: for answer with correct reasoning (no single points given)

Task 5 Physics

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Task 5.1 General questions

A) Name two kinds of wirebased electrical media that can provide protection against crosstalk. Explain shortly how interferences can be eliminated in these. 2

Twisted Pair: Due to the twisting interferences have the same impact on both wires and can be eliminated by using the difference.

Coaxial Cable: Advantage because of electromagnetic shielding by the conducting sheath that prevent most interferences like a cage of Faraday.

Ribbon Cable: Here the wires are close to each other so cross talking happens easily. To minimise interferences a ground wire can be places between two signal wires.

1 pt per name including explanation (2 pt max)

B) Explain the the basic working principal of bus drivers based on Tristate Gates and Open Collector based bus drivers. Discuss the advantages and disadvantages for both driver variants. 3

Tristate gate

- Parallel switching of several outputs is not possible with simple TTL gates: danger of short-circuit
- By turning off unused output stages, several of such circuits can be connected to one bus
- Third state (Tristate): high-resistance (Z)
- In each case only one output is allowed to drive the bus, all others must show high-resistance

Open collector bus

- The collector of each of the output transistors remains unconnected
- All bus members share one collector resistor
- The output is only then HIGH if all transistors cut off
- low value (GND) on the bus line is dominant value

0.5 pt per headword; max. 1.5 pt per bus driver (3 of 4 is enough)

C) Explain TTL-Level and the different High/Low thresholds. 1

Valid HIGH and LOW areas are wider at the input due to possible voltage drops on the lines

Asymmetric division since the HIGH level drops under load which does not happen to the LOW level

1 pt: acceptance bands explanation
(0,5 pts are not given!)

Task 5.2 Sampling

A) What is necessary to fully reconstruct an analog signal when sampling it of a physical medium? How are artefacts avoidable? **2**

$$f_{sample} \geq 2 * f_{max}$$

A continuous signal has to be sampled with a frequency at least double the maximum frequency of the signal itself f_{max} order to be able to unambiguously reconstruct the original signal.

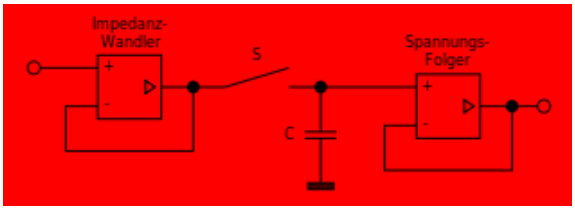
Sampling at equidistant time points.

No quantization of sampled value

A: 1 pt for correct explanation and equation
B: 1 pt for "low-pass-filter"

To avoid aritfacts it may be necessary to filter the signal prior to sampling with a low-pass filter. This prevents artefacts otherwise caused by high frequencies.

B) Draw a Sample&Hold. Why are they needed for A/D-conversion? **4**



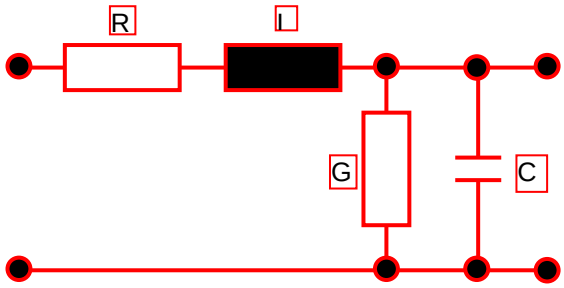
Analogue signals change over time. Because of this analog signals have to be kept constant for the duration of analog-digital conversion.

A: 3pt: Drawing
(1 pt: "Impedanzwandler"
1 pt: "Spannungsfolger"
1 pt: "S + C")
B: 1 pt for explanation

Task 5.3 Model of Signal Lines

How are long signal lines modeled? Draw the equivalent circuit diagram of a long line. Explain why and how it is used. Give the formula for the impedance (loss-less case).

3



Long signal lines are described using a distributed waveguide model with a series of RLC quadripoles

It can be calculated for lossless signal lines from the distributed capacities and inductances per length

Impedance: $Z_W = \sqrt{\frac{L'}{C'}}$

Drawing:
A: +2 pt: correct circuit diagram (0.5 pt per element at correct position)

B: +0.5 pt: explanation (series of quadpole to model complete line)
C: +0.5 pt: for correct formula

Task 5.4 Reflection on wires

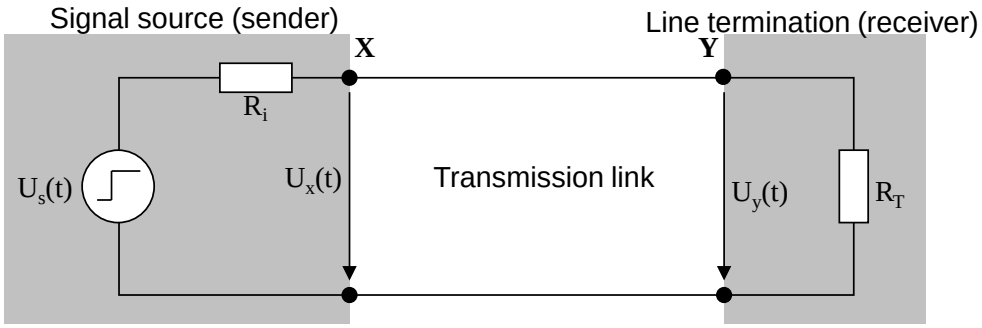


Figure 5.1: Test Setup

A) In Figure 5.1 an assembly is considered, consisting of a voltage source with an internal resistance R_i = 600Ω as sender and a receiver with R_T = 300Ω. The DC resistance of the line is zero. Calculate the value of the wave resistance at the time of t=0. **2**

At the time t=0 the voltage U_s of the sender changes from 0V to 5V and is constant afterwards. The propagation time of a wave on the wire is t_d. The voltage u_x at the time of t=0 is $U_x(0)$=3V.

$$u_x(0) = u_s \cdot \frac{Z_w}{R_i + Z_w}$$

$$Z_w = \frac{\frac{u_x(0)}{u_s} R_i}{1 - \frac{u_x(0)}{u_s}} = \frac{\frac{3V}{5V} 600\Omega}{1 - \frac{3V}{5V}} = 900\Omega$$

1 pt for correct equation
1 pt for correct result

B) Calculate the reflection factors on both sides of the test setup in Figure 5.1. **2**

$$End\ of\ wire: r_e = \frac{R_T - Z_w}{R_T + Z_w} = \frac{300\Omega - 900\Omega}{300\Omega + 900\Omega} = -0{,}5$$

$$Begin\ of\ wire: r_s = \frac{R_i - Z_w}{R_i + Z_w} = \frac{600\Omega - 900\Omega}{600\Omega + 900\Omega} = -0{,}2$$

0.5 pt for each correct equation
0.5 pt for each correct result
"Folgefehler" from previous task possible

C) Which voltage value appears at the points X and Y after t = 1? **1**

$$Voltage\ at\ point\ Y: u_y(t) = u_x(t-1) + r_e \cdot \lfloor u_x(t-1) - u_y(t-2) \rfloor$$

$$Voltage\ at\ point\ X: u_x(t) = u_y(t-1) + r_s \cdot \lfloor u_y(t-1) - u_x(t-2) \rfloor$$

$$U_x(0) = 3V$$

$$U_y(0) = 0V$$

$$U_y(1) = 1{,}5\ V$$

$$U_x(1) = 3V$$

0.5 pt for correct equation
0.5 pt for correct result

"Folgefehler" from previous task possible due to other reflection factor

D) Which voltage value appears at the points X and Y after an infinite amount of time and why?

2

After an infinite amount of time the system is in a steady state, the voltages at points X and Y are identical. When neglecting the DC resistance of the wire a series connection of R_i and R_T remains.

$$u_x(\infty) = u_y(\infty) = u_s \cdot \frac{R_T}{R_T + R_i} = 5V \cdot \frac{300}{300 + 900} = 1{,}67V$$

1 pt for correct explanation
0.5 pt for correct equation
0.5 pt for correct result

Task 6 Practical Aspects of Communication Systems

16

Task 6.1 General Questions

A) Name 4 multi master capable bus systems:

1

CAN

FlexRay

I^2C

FireWire

PCI

1 pt: 4 correct bus systems

OR

0,5 pt: 3 correct bus systems system

1

B) Briefly describe the difference between isochronous transmission and bulk transfers of the USB specification:

Isochronous transmission: Fixed data rate, no error handling, e.g. for video transmission.

Bulk-transfer: For large amounts of data, long waiting time possible, error correction, e.g. for USB storage devices

C) Name 3 advantages of CAN over USB:

1

Multiple masters possible

Prioritization of messages

Multicast

Node is allowed to send as soon as the physical transmission medium is free Shorter bus access latency and transmission time

1 pt: 3 correct advantages

OR

0,5 pt: 2 correct advantages

1

D) Name 3 advantages of USB over CAN

Hot plug capable

Higher bandwidth than CAN

Power supply over bus

Autonegotiation of transmission speed

Larger packet size / less overhead for large amounts of data

1 pt: 3 correct advantages

OR

0,5 pt: 2 correct advantages

Task 6.2 USB Protocol

Design an USB topology with the given minimal bandwidth requirements for the devices listed in table 2. For cost reasons use the lowest possible USB mode for each connection. All USB modes are listed in table 1 as a reference.

Table 1: Reference of USB modes

USB Mode	Shortcut	Max. Bandwidth	USB Generation
Low Speed	LS	1.5 Mbit/s	USB-1
Full Speed	FS	12.5 Mbit/s	USB-1
Hi-Speed	HS	480 Mbit/s	USB-2
SuperSpeed	SS	5 Gbit/s	USB-3

A) Fill out the column for USB generation / mode of table 2 with the minimal needed USB mode and it's corresponding generation for the given devices and their maximum data rate. **3**

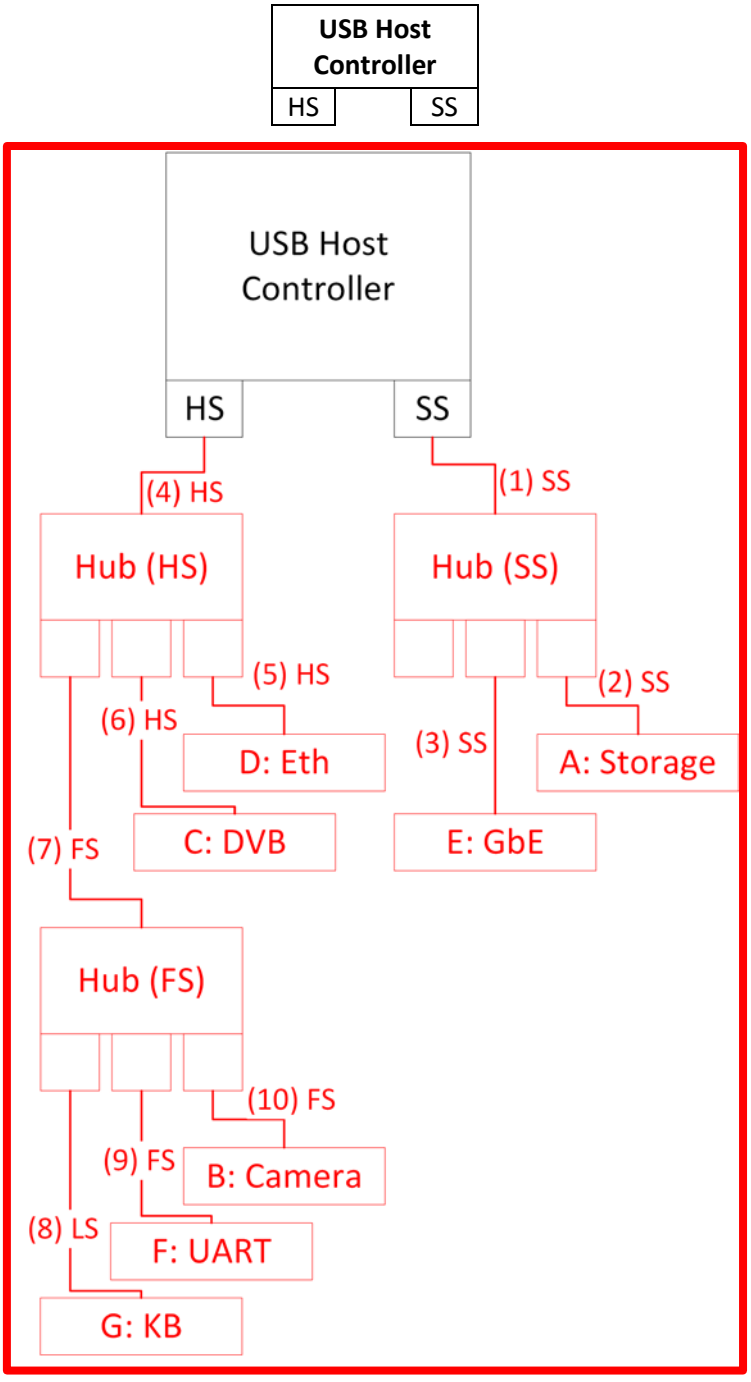
Table 2: USB Devices to use

Name	Device	Max. Data Rate of Device	USB Gen. / Mode
A	USB Storage Device	640 Mbit/s	USB-3 SS
B	USB Camera Device	5 Mbit/s	USB-1 FS
C	DVB Video Receiver	15 Mbit/s	USB-2 HS
D	Fast Ethernet Controller	100 Mbit/s	USB-2 HS
E	Gigabit Ethernet Controller	1 Gbit/s	USB-3 SS
F	USB to Serial Adapter with 1.5 Mbit/s UART	1.5 Mbit/s	USB-1 FS
G	USB Keyboard	8 Kbit/s	USB-1 LS

-0.5 pt for each wrong row

The USB host controller has 1 port supporting LS, FS, HS and SS modes and 1 port supporting LS, FS and HS modes. 1 USB-3 hub, 1 USB-2 hub and 1 USB-1 hub with **3 ports each** are available.

B) Draw the topology tree with all devices of table 2 and the above listed hubs. Tag every connection (bus segment) with an identifier / number and the USB mode you chose. **4**



-0.5 pt for wrong node (hub or device)
-0.5 pt for wrong connection with mode annotation

C) Calculate the bandwidth utilization for each bus segment of your topology, if all devices are operating at their full speed. Assume a general protocol overhead of 20 %. Give all steps of your solution and use your assigned identifier.

4

U(2) = 640 Mbit/s * 1.2 / (5 Gbit/s) = 15 %
U(3) = 1 Gbit/s * 1.2 / (5 Gbit/s) = 24 %
U(1) = U(2) + U(3) = 39 %

U(5) = 100 Mbit/s * 1.2 / (480 Mbit/s) = 25 %
U(6) = 15 Mbit/s * 1.2 / (480 Mbit/s) = 3.75 %

U(8) = 8 Kbit/s * 1.2 / (1.5 Mbit/s) = 0.625 %
U(9) = 1.5 Mbit/s * 1.2 / (12 Mbit/s) = 15 %
U(10) = 5 Mbit/s * 1.2 / (12 Mbit/s) = 50 %
U(7) = U(8) + U(9) + U(10) = 65.625 %

U(4) = ([U(5) + U(6) * 480 Mbit/s] + [U(7) * 12 Mbit/s]) / (480 Mbit/s) = 30.39 %

-0.5 pt for each wrong utilization
- 1 pt if utilization is not given as a percentage

D) An USB topology should be used in a partly real-time capable environment. One connected device has hard real-time requirements and therefore guaranteed latencies have to be ensured. Is this possible with an USB topology? Justify your answer.

1

Yes, because the host controller is polling every subscriber and USB supports fixed data rates using the isochronous transmission mode.

Point only given with correct reasoning (no half points possible)

Task 7 Networks

13

Task 7.1 OSI Reference Model

Figure 7-1 shows the 7 layers and the layer names of the OSI reference model

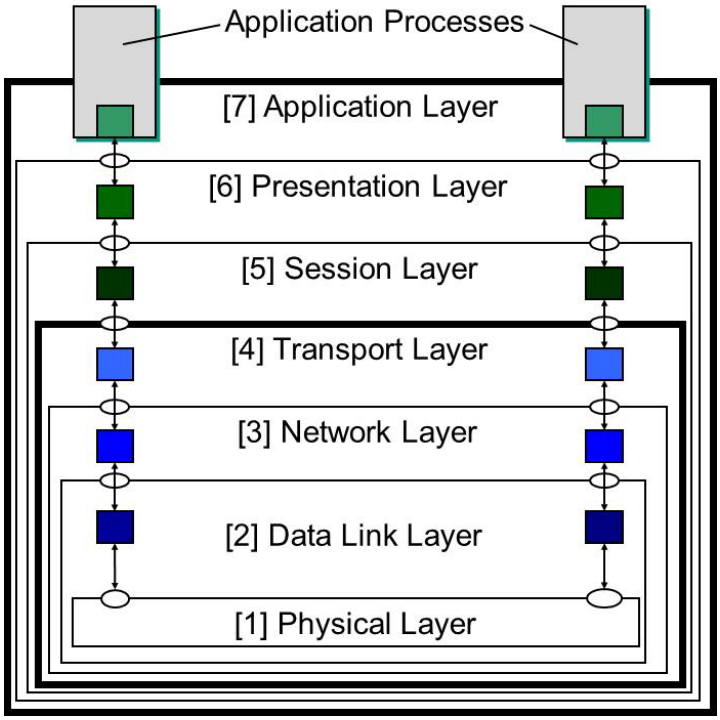


Figure 7-1: The 7 Layers of the OSI reference model

When communicating through a network, typically the application used in the end-node (e.g. personal computer), the operating system (OS) of the end-node, the hardware of the node and the switching components of the network are involved.

A) Mark all layers (with an X), that are realized by the respective component

1

Component	OSI Layer						
	1	2	3	4	5	6	7
Repeater	X						
Bridge	X	X					
Router	X	X	X				
Gateway	X	X	X	X	(X)	(X)	(X)
Smartphone/Server	X	X	X	X	X	X	X

Point only given for correct table (no half points possible)

B) Give one specific example (protocol, application …) for each layer of the internet reference model. **1**

Application Layer: HTTP, IMAP, FTP, DNS, POP3

Transport Layer: TCP, UDP

Internet Layer: Internet Protocol (IPv4, IPv6), ICMP

Network Layer: Ethernet, WLAN (802.11x), Token Bus/Ring, FDDI

Point only given for correct example in all layers (no half points possible)

C) What are the main differences between the OSI-reference model and the Internet reference model (Give at least two points.) **2**

1. In the internet-reference model, tasks of OSI-layers 5 und 6 are moved completely into the application layer
2. OSI-layers 1 and 2 are combined to a single layer
3. TCP/IP supports two transport protocols: TCP (connection-orientated) and UDP (connection less)

A: 1pt: combination of layers into one
B: 1pt: What layers are combined? (at least one example)

Task 7.2 Routing

A) What is the task of a routing mechanism **1**

Decide about the way to be used by the packet on its way through the Network

From the perspective of a single router/distributed routing: To decide which output port is used by the packet

B) Why is adaptive routing referred to be more flexible than static routing **1**

Routing information are computed at run-time taking the network status

Information into account

Figure 7-2 shows a 4x4 meshed network with bidirectional links for wormhole packet-switching communication.

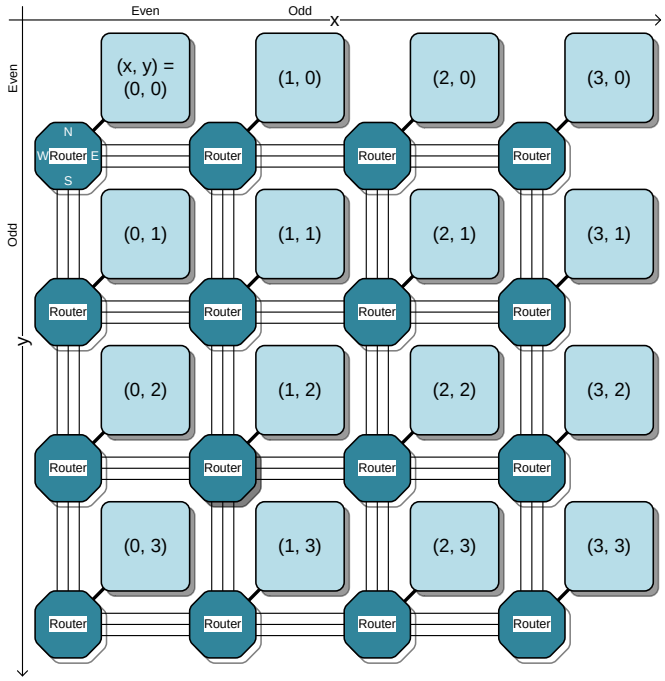


Figure 7-2: 4x4 meshed network

C) Which routers are passed by a packet sent from (x, y) = (0, 1) to (3, 3) using XY-Routing. Please provide the coordinates of the passed router in the order given by the transmission process. **1**

(0, 1), (1, 1), (2, 1), (3, 1), (3, 2), (3, 3)

D) Give a valid minimal path for a packet sent from (x, y) = (1, 1) to (3, 2) using Odd-Even-Turn Routing (only definition from CSP lecture is valid). Please provide the coordinates of the passed router in the order given by the transmission process. **1**

(1, 1), (2, 1), (3, 1), (3, 2) OR (1, 1), (1, 2), (2, 2), (3, 2)

OR (1, 1), (2, 1), (2, 2), (3, 2)

E) Is there an invalid but minimal path for the transmission conditions, defined in D)? Justify your answer. **1**

There is no minimal path, which is invalid.

Reason: There are no turns from an East-Port and no turns to a West port that could violate any of the odd-even rules.

1pt: given only with correct reason

Task 7.3 Packet- vs. Circuit-Switching

The following table defines the properties of a packet- and a circuit-switching network.

Property	**Packet-Switching Network**	**Circuit-Switching Network**
Connection Setup Time	0 us (no setup required)	27 us
Max. Packet Size	100 flits	Arbitrary (not limited)
Packet Delay	100 $\frac{ns}{flit}$ * #flit + 1 us	10 $\frac{ns}{flit}$ * #flit
Energy Consumption (Setup)	0 $\frac{uJ}{flit}$	1 $\frac{uJ}{flit}$
Energy Consump. (Transmission)	20 $\frac{nJ}{flit}$	2 $\frac{nJ}{flit}$

For a specific application, a dataset of 250 flits needs to be transmitted to the same receiver. Subsequently a new receiving node is selected for the next transmission.

Which network is to be more appropriate for this scenario? Justify your answer analytically!

A) The latency is the primary optimization goal: **2**

Packet-switching:

$2 * (100 \frac{ns}{flit} * 100 \text{ flit} + 1 \text{ us}) + (100 \frac{ns}{flit} * 50 \text{ flit} + 1 \text{ us}) = 28 \text{ us}$

Circuit-switching:

$27 \text{ us} + (10 \frac{ns}{flit} * 250 \text{ flit}) = 29.5 \text{ us}$

⇨ There is a small advantage for the packet switching network. It provides a lower latency for the given scenario.

1pt: Ansatz via calculation of latencies
1pt: correct calculation and reasoning
(No half points!)

B) Energy consumption the primary optimization goal: **2**

Packet-switching:

$20 \frac{nJ}{flit} * 250 \text{ flit} = 5 \text{ uJ}$

Circuit-switching:

$1 \frac{uJ}{flit} + 2 \frac{nJ}{flit} * 250 \text{ flit} = 1{,}5 \text{ uJ}$

⇨ The circuit switching network has a clear advantage with respect to power consumption.

C)
A: 1pt: Ansatz via calculation of energy consumption
B: 1pt: correct calculation and reasoning